What Is Claimed Is:

1. An arrangement of differential pairs of wires that carry differential signals across a semiconductor chip, comprising:

a set of parallel tracks on the semiconductor chip that are used to route the differential pairs of wires;

wherein each differential pair of wires includes a true wire and a complement wire that carry corresponding true and complement signals;

wherein the differential pairs of wires are non-adjacent, so that each true wire is separated from its corresponding complement wire by at least one intervening wire in the set of parallel tracks, thereby reducing coupling capacitance between corresponding true and complement wires; and

one or more twisting structures, wherein a twisting structure twists a differential pair of wires so that the corresponding true and complement wires are interchanged within the set of parallel tracks.

2. The arrangement of claim 1, wherein the one or more twisting structures are arranged so that substantially zero net differential coupling capacitance exists for each differential pair of wires.

3. The arrangement of claim 2,

wherein the set of parallel tracks includes a possibly repeating pattern of four adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track;

wherein the differential pairs of wires include a first differential pair, A and $\overline{A}$, and a second differential pair, B and $\overline{B}$;

wherein A starts in the first track, B starts in the second track, $\overline{A}$ starts in the third track and $\overline{B}$ starts in the fourth track;

wherein a first twisting structure causes B and $\overline{B}$ to interchange, so that A is in the first track, $\overline{B}$ is in the second track, $\overline{A}$ is in the third track and B is in the fourth track;

wherein a second twisting structure causes A and $\overline{A}$ to interchange, so that $\overline{A}$ is in the first track, $\overline{B}$ is in the second track, A is in the third track and B is in the fourth track; and

wherein a third twisting structure causes $\overline{B}$ and B to interchange, so that $\overline{A}$ is in the first track, B is in the second track, A is in the third track and $\overline{B}$ is in the fourth track.

4. The arrangement of claim 3,

wherein the first twisting structure is located approximately one quarter of the way down the set of parallel tracks;

wherein the second twisting structure is located approximately one half of the way down the set of parallel tracks; and

wherein the third twisting structure is located approximately three quarters of the way down the set of parallel tracks.

5. The arrangement of claim 3,

wherein the first twisting structure is located more than one quarter of the way down the set of parallel tracks;

wherein the second twisting structure is located more than one half of the way down the set of parallel tracks; and

wherein the third twisting structure is located more than three quarters of the way down the set of parallel tracks.

6. The arrangement of claim 2,

wherein the set of parallel tracks includes a possibly repeating pattern of four adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track;

wherein the differential pairs of wires include a first differential pair, A and $\overline{A}$, and a second differential pair, B and $\overline{B}$;

wherein A starts in the first track, B starts in the second track, $\overline{A}$ starts in the third track and $\overline{B}$ starts in the fourth track; and

wherein a first twisting structure causes A and $\overline{A}$ to interchange, so that $\overline{A}$ is in the first track, B is in the second track, A is in the third track and $\overline{B}$ is in the fourth track.

7. The arrangement of claim 6, wherein the first twisting structure is located approximately one half of the way down the set of parallel tracks.

8. The arrangement of claim 6, wherein the first twisting structure is located more than one half of the way down the set of parallel tracks.

9. The arrangement of claim 2,

wherein the set of parallel tracks includes a possibly repeating pattern of six adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track, which is adjacent to a fifth track, which is adjacent to a sixth track;

wherein the differential pairs of wires include a first differential pair, A and $\overline{A}$, a second differential pair, B and $\overline{B}$, and a third differential pair, C and $\overline{C}$;

wherein A starts in the first track, B starts in the second track, $\overline{A}$ starts in the third track, C starts in the fourth track, $\overline{B}$ starts in the fifth track and $\overline{C}$ starts in the sixth track; and

wherein a first twisting structure causes A and $\overline{A}$ to interchange, so that $\overline{A}$ is in the first track, B is in the second track, A is in the third track, C is in the fourth track, $\overline{B}$ is in the fifth track and $\overline{C}$ is in the sixth track.

10. The arrangement of claim 9, wherein the first twisting structure is located approximately one half of the way down the set of parallel tracks.

11. The arrangement of claim 9, wherein the first twisting structure is located more than one half of the way down the set of parallel tracks.

12. The arrangement of claim 1,

wherein the set of parallel tracks are located within the same metal layer in the semiconductor chip; and

wherein the one or more twisting structures use at least one other metal layer to interchange signals between tracks.

13. A method for arranging differential pairs of wires to carry differential signals across a semiconductor chip, wherein each differential pair of wires includes a true wire and a complement wire that carry corresponding true and complement signals, the method comprising:

defining a set of parallel tracks on the semiconductor chip, which are used to route the differential pairs of wires;

mapping differential pairs of wires to tracks so that the differential pairs of wires are non-adjacent, which means that each true wire is separated from its corresponding complement wire by at least one intervening wire in the set of parallel tracks, thereby reducing coupling capacitance between corresponding true and complement wires; and

locating one or more twisting structures, wherein a twisting structure twists a differential pair of wires so that the corresponding true and complement wires are interchanged within the set of parallel tracks.

14. The method of claim 13, wherein the one or more twisting structures are located so that substantially zero net differential coupling capacitance exists for each differential pair of wires.

15. The method of claim 14,

wherein the set of parallel tracks includes a possibly repeating pattern of four adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track;

wherein the differential pairs of wires include a first differential pair, A and $\overline{A}$, and a second differential pair, B and $\overline{B}$;

wherein A starts in the first track, B starts in the second track, $\overline{A}$ starts in the third track and $\overline{B}$ starts in the fourth track;

wherein a first twisting structure causes B and $\overline{B}$ to interchange, so that A is in the first track, $\overline{B}$ is in the second track, $\overline{A}$ is in the third track and B is in the fourth track;

wherein a second twisting structure causes A and $\overline{A}$ to interchange, so that $\overline{A}$ is in the first track, $\overline{B}$ is in the second track, A is in the third track and B is in the fourth track; and

wherein a third twisting structure causes $\overline{B}$ and B to interchange, so that $\overline{A}$ is in the first track, B is in the second track, A is in the third track and $\overline{B}$ is in the fourth track.

16. The method of claim 14,

wherein the set of parallel tracks includes a possibly repeating pattern of four adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track;

wherein the differential pairs of wires include a first differential pair, A and $\overline{A}$, and a second differential pair, B and $\overline{B}$;

wherein A starts in the first track, B starts in the second track, $\overline{A}$ starts in the third track and $\overline{B}$ starts in the fourth track; and

wherein a first twisting structure causes A and $\overline{A}$ to interchange, so that $\overline{A}$ is in the first track, B is in the second track, A is in the third track and $\overline{B}$ is in the fourth track.

17. The method of claim 14,

wherein the set of parallel tracks includes a possibly repeating pattern of six adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track, which is adjacent to a fifth track, which is adjacent to a sixth track;

wherein the differential pairs of wires include a first differential pair, A and $\overline{A}$, a second differential pair, B and $\overline{B}$, and a third differential pair, C and $\overline{C}$;

wherein A starts in the first track, B starts in the second track, $\overline{A}$ starts in the third track, C starts in the fourth track, $\overline{B}$ starts in the fifth track and $\overline{C}$ starts in the sixth track; and

wherein a first twisting structure causes A and $\overline{A}$ to interchange, so that $\overline{A}$ is in the first track, B is in the second track, A is in the third track, C is in the fourth track, $\overline{B}$ is in the fifth track and $\overline{C}$ is in the sixth track.

18. An arrangement of differential pairs of wires that carry differential signals across a semiconductor chip, comprising:

a set of parallel tracks on the semiconductor chip that are used to route the differential pairs of wires;

wherein each differential pair of wires includes a true wire and a complement wire that carry corresponding true and complement signals;

wherein the differential pairs of wires are non-adjacent, so that each true wire is separated from its corresponding complement wire by at least one intervening wire in the set of parallel tracks, thereby reducing coupling capacitance between corresponding true and complement wires; and

one or more twisting structures, wherein a twisting structure twists a differential pair of wires so that the corresponding true and complement wires are interchanged within the set of parallel tracks, and wherein the one or more twisting structures are arranged so that substantially zero net differential coupling capacitance exists for each differential pair of wires;

wherein the set of parallel tracks includes a possibly repeating pattern of four adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track;

wherein the differential pairs of wires include a first differential pair, A and $\overline{A}$, and a second differential pair, B and $\overline{B}$;

wherein A starts in the first track, B starts in the second track, $\overline{A}$ starts in the third track and $\overline{B}$ starts in the fourth track;

wherein a first twisting structure causes B and $\overline{B}$ to interchange, so that A is in the first track, $\overline{B}$ is in the second track, $\overline{A}$ is in the third track and B is in the fourth track;

wherein a second twisting structure causes A and $\overline{A}$ to interchange, so that $\overline{A}$ is in the first track, $\overline{B}$ is in the second track, A is in the third track and B is in the fourth track; and

wherein a third twisting structure causes $\overline{B}$ and B to interchange, so that $\overline{A}$ is in the first track, B is in the second track, A is in the third track and $\overline{B}$ is in the fourth track.

19. An arrangement of differential pairs of wires that carry differential signals across a semiconductor chip, comprising:

a set of parallel tracks on the semiconductor chip that are used to route the differential pairs of wires;

wherein each differential pair of wires includes a true wire and a complement wire that carry corresponding true and complement signals;

wherein the differential pairs of wires are non-adjacent, so that each true wire is separated from its corresponding complement wire by at least one

intervening wire in the set of parallel tracks, thereby reducing coupling capacitance between corresponding true and complement wires; and

one or more twisting structures, wherein a twisting structure twists a differential pair of wires so that the corresponding true and complement wires are interchanged within the set of parallel tracks, and wherein the one or more twisting structures are arranged so that substantially zero net differential coupling capacitance exists for each differential pair of wires;

wherein the set of parallel tracks includes a possibly repeating pattern of four adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track;

wherein the differential pairs of wires include a first differential pair, A and $\overline{A}$, and a second differential pair, B and $\overline{B}$;

wherein A starts in the first track, B starts in the second track, $\overline{A}$ starts in the third track and $\overline{B}$ starts in the fourth track; and

wherein a first twisting structure causes A and $\overline{A}$ to interchange, so that $\overline{A}$ is in the first track, B is in the second track, A is in the third track and $\overline{B}$ is in the fourth track.

20. An arrangement of differential pairs of wires that carry differential signals across a semiconductor chip, comprising:

a set of parallel tracks on the semiconductor chip that are used to route the differential pairs of wires;

wherein each differential pair of wires includes a true wire and a complement wire that carry corresponding true and complement signals;

wherein the differential pairs of wires are non-adjacent, so that each true wire is separated from its corresponding complement wire by at least one

intervening wire in the set of parallel tracks, thereby reducing coupling capacitance between corresponding true and complement wires; and

one or more twisting structures, wherein a twisting structure twists a differential pair of wires so that the corresponding true and complement wires are interchanged within the set of parallel tracks, and wherein the one or more twisting structures are arranged so that substantially zero net differential coupling capacitance exists for each differential pair of wires;

wherein the set of parallel tracks includes a possibly repeating pattern of six adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track, which is adjacent to a fifth track, which is adjacent to a sixth track;

wherein the differential pairs of wires include a first differential pair, A and $\overline{A}$, a second differential pair, B and $\overline{B}$, and a third differential pair, C and $\overline{C}$;

wherein A starts in the first track, B starts in the second track, $\overline{A}$ starts in the third track, C starts in the fourth track, $\overline{B}$ starts in the fifth track and $\overline{C}$ starts in the sixth track; and

wherein a first twisting structure causes A and $\overline{A}$ to interchange, so that $\overline{A}$ is in the first track, B is in the second track, A is in the third track, C is in the fourth track, $\overline{B}$ is in the fifth track and $\overline{C}$ is in the sixth track.

21. An arrangement of differential pairs of wires that carry differential signals across a semiconductor chip, comprising:

a set of parallel tracks on the semiconductor chip that are used to route the differential pairs of wires;

wherein each differential pair of wires includes a true wire and a complement wire that carry corresponding true and complement signals; and

wherein the differential pairs of wires are non-adjacent, so that each true wire is separated from its corresponding complement wire by at least one intervening wire in the set of parallel tracks, thereby reducing coupling capacitance between corresponding true and complement wires.

22. The arrangement of differential pairs of wires of claim 21,

wherein the set of parallel tracks includes a possibly repeating pattern of four adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track;

wherein the differential pairs of wires include a first differential pair, A and $\overline{A}$, and a second differential pair, B and $\overline{B}$; and

wherein A resides in the first track, B resides in the second track, $\overline{A}$ resides in the third track and $\overline{B}$ resides in the fourth track.

23. A method for arranging differential pairs of wires to carry differential signals across a semiconductor chip, wherein each differential pair of wires includes a true wire and a complement wire that carry corresponding true and complement signals, the method comprising:

defining a set of parallel tracks on the semiconductor chip, which are used to route the differential pairs of wires; and

mapping differential pairs of wires to tracks so that the differential pairs of wires are non-adjacent, which means that each true wire is separated from its corresponding complement wire by at least one intervening wire in the set of parallel tracks, thereby reducing coupling capacitance between corresponding true and complement wires.

24. The method of claim 23,

wherein the set of parallel tracks includes a possibly repeating pattern of four adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track;

wherein the differential pairs of wires include a first differential pair, A and $\overline{A}$, and a second differential pair, B and $\overline{B}$; and

wherein A resides in the first track, B resides in the second track, $\overline{A}$ resides in the third track and $\overline{B}$ resides in the fourth track.